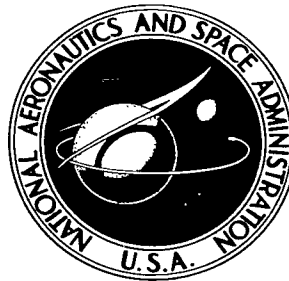


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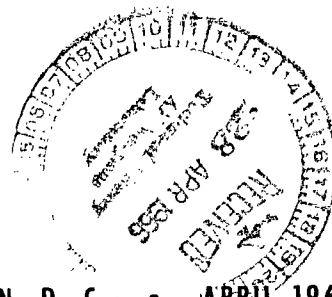
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INTEGRATED TELEMETRY-COMPUTER SYSTEM

by Donald E. Jamison
Goddard Space Flight Center
Greenbelt, Md.



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INTEGRATED TELEMETRY-COMPUTER SYSTEM

By Donald E. Jamison

Goddard Space Flight Center
Greenbelt, Md.

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ABSTRACT

This paper discusses the feasibility of integrating a high speed, general purpose, small scale, digital computer with a pulse frequency modulation signal reduction and conversion system in order to obtain the highest quality of intelligence in a minimum period of time.

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INTEGRATED TELEMETRY-COMPUTER SYSTEM

by

Donald E. Jamison

Goddard Space Flight Center

INTRODUCTION

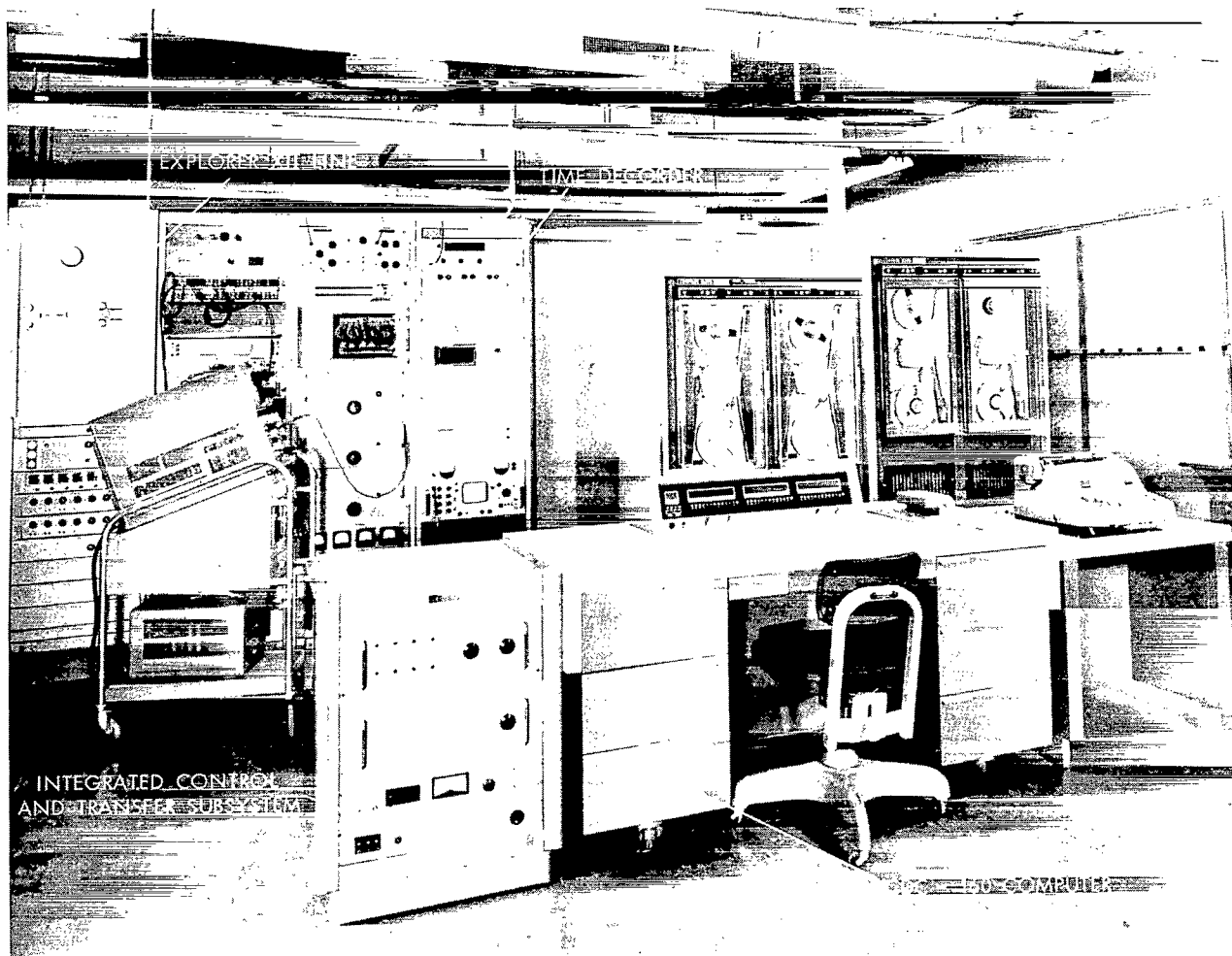
A design project was undertaken and completed to determine the feasibility of integrating a high speed, general purpose, small scale, digital computer with a telemetry signal acquisition and conversion system. The computer selected was the CDC 160 manufactured by the Control Data Corp. The telemetry signal acquisition and conversion system consists of the pulse-frequency-modulation (PFM) data processor for the Explorer XII satellite (1961 v 1). The time decoder converts standard NASA time codes to digital format. The latter two pieces of equipment were constructed at NASA. The integrated system is shown in Figure 1.

A block diagram of the former data processing method is shown in Figure 2. The illustration shows the transmission of information, i.e., the data flow, as it passes through the signal acquisition and processing stage to storage and then out for further data reduction. The vertical lines divide the process into three time periods. The time between the lines is a variable dependent upon scheduling sophistication and production control of the data processing operation.

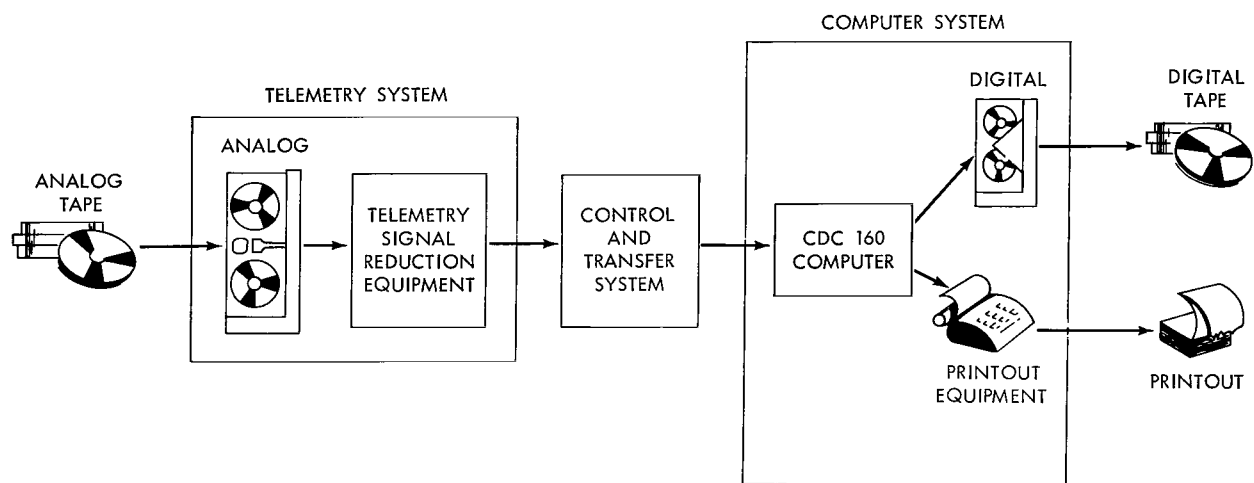
The previous processing method was as follows. After tape evaluation, the analog tapes received from the satellite data acquisition network were played back and converted from analog-to-digital information in the telemetry signal processing line. The digital information was then edited and formatted by special purpose buffering devices and stored on magnetic tapes in IBM format. Following this procedure, further editing of the tape was performed on a medium size, general purpose computer.

It can be observed that the system involves physical handling of data tapes during both analog-to-digital conversion and computer editing. The procedure requires expenditures of time and manpower that can be saved by taking advantage of the time available between signal inputs during the analog-to-digital conversion periods. Use of advanced design techniques accomplishes savings in time and manpower.

In the telemetry processing system mentioned, the equipment that performs the digital recording and formatting can be considered as a special purpose computer that has the ability to perform



(a) Photograph of system



(b) Equipment relationship

Figure 1-Integrated telemetry-computer system.

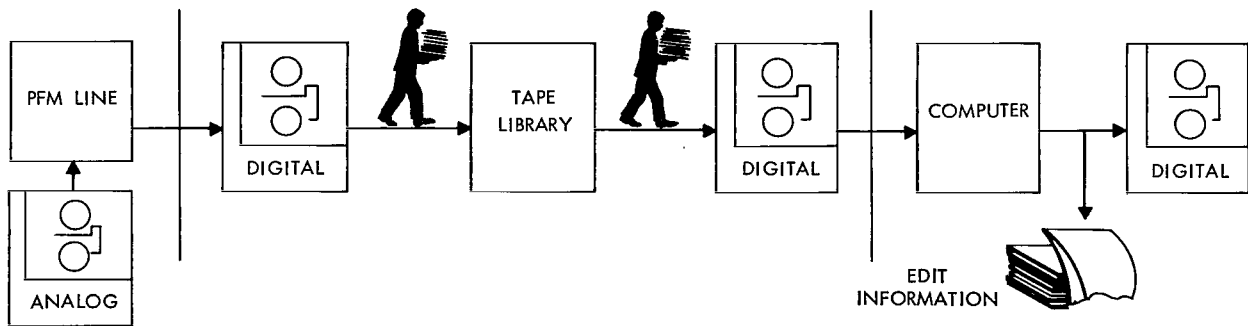


Figure 2-Former processing method.

a limited number of functions rapidly. However, the digital information that is recorded by this equipment must be transferred to a high speed, general purpose computer for further editing and formatting. Application of suitable design techniques can therefore introduce an economy of operation in the system. There are many types of general purpose computers that can be integrated into an overall system to accomplish this task. During the time the signal conversion is occurring, other functions can also be performed. Available time is fully used and the data processing operation approaches its desired goal of obtaining the highest quality of data in the shortest period of time. The final result is a savings in equipment and in manpower, a considerable reduction in total processing time, and a more expedient and efficient system. It was with this concept in mind that a program of integrating a computer into a telemetry reduction system was initiated. The proposed equipment relationship for the integrated telemetry-computer system is shown in Figure 1 (b).

SYSTEM DESIGN

Initial Design Concept

The initial design concept was based upon economy of construction as a main factor along with the following constraints. No changes would be made to either the circuits within the CDC-160 computer proper or the external commercial equipment which served as standard input/output devices.

The first prototype used the output storage register of the Explorer XII PFM telemetry acquisition and conversion line as the data transfer element to the computer. A flexible simulator was also constructed to transfer test data to the computer at a predetermined rate. This simulator was designed so that the computer could be used in both a single instruction progression and a continuous highspeed operational mode for test purposes.

Various input and editing programs were performed by the computer in periods ranging from several microseconds to a few milliseconds. These routines allowed the computer to accept inputs and execute information checks easily.

The incorporation of an interlaced output program after the data had been edited and stored proved to be unsuccessful. The computer was able to reference and readily dispose of information, but the mechanical and electronic control features of the magnetic tape units were too slow to permit the computer to accept another input word during the time the output routine was occurring. In this case, the use of a single transfer register to transmit information into the computer proved to be inadequate because of a slow tape drive turn-on response. Consequently, the initial design concept had to be reconsidered. The results of continued testing indicated further considerations when using a nonbuffered computer. A computer without simultaneous input-output capability is constricted in its operations by the functions of the external equipment. Even if the desired operations of entering, computing, and passing information had been accomplished successfully in the initial approach, it still would not have been feasible to speed up input data without adding external hardware as well as modifying the system program routines. This inadequacy and the compensating modifications are eliminated by the use of a similar computer with a buffering channel for input/output operations.

Final Design Concept

The final design alleviated the conditions imposed by the external equipment in the initial design. A different and more complex interfacing transfer and control mechanism had to be developed in order to solve the problems mentioned in the preceding section. Since the limitations of the single transfer register made it impossible to store the telemetry input data for any significant time period, an interface device that would also store data temporarily was finally decided upon.

The final design concept decreases the data input rate to the computer and thereby increases the time period for each input word so that the output of information can be performed with sufficient time for computation as well as a return to an input mode. This redesign provides a more flexible system than the initial design. The sacrifice in the economy of construction and the increased number of information storage circuits was well justified. In the final design concept, the data input can be handled easily at the nominal rate. Control arrangements are such that data can be transferred and processed at twice the nominal rate. With these improved features, the final system was more than able to meet the project operation requirements.

The programming was also simplified in the redesign by omitting routines to compensate for the close timing tolerances that were initially experienced. Consequently, it is easier to test the system during operational checkouts.

A simulator was constructed for the first system because of the unavailability of an analog-to-digital reduction line for experimentation. Although the simulator was satisfactory for its initial application, it was reconstructed for the second design and is now far less complex. Computer-simulator control generation circuits were also added to the second design. The simulation circuits are contained in a separate cabinet with the rest of the interfacing transfer and control circuits. The simulator will test the system for information passage, storage register reliability, and control timing.

TECHNICAL DESIGN

Integrated Telemetry-Computer System

Figure 3 is a block diagram of the integrated telemetry-computer system illustrating how the CDC 160 computer is connected to the telemetry processor. The integrated control and transfer system regulates the data processing flow from the processor to the computer. Its two main functions are to synchronize the control pulses between the processing equipment and the computer, and to accept information from the telemetry system and hold it until the computer requests it. The integrated control and transfer unit is positioned outside the CDC 160 computer.

The integrated telemetry-computer system consists of the Explorer XII telemetry processing line, the CDC 160 computer with its peripheral equipment, and a binary coded decimal (BCD) time decoder. The main parameters and the essential characteristics of the subsystems are as follows:

Explorer XII satellite telemetry processor:

1. Processes PFM data, 5 kc to 15 kc
2. 128-comb filter bank, 114 filters utilized
3. 13-bit digital output register
4. Digital count, 115 maximum
5. Octal count, 700 maximum
6. Most significant bit, bad data flag
7. 16-channel decommutation
8. Data word rate, 20 milliseconds
9. Frame rate, 320 milliseconds
10. Output control signals
 - a. Data present
 - b. Time hold, time statisize
 - c. Time present

Time decoder:

1. BCD time output used, 4 bits per character
2. 12 time characters

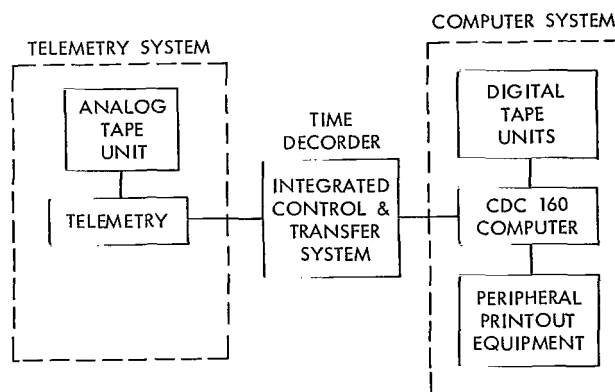


Figure 3-Block diagram of integrated telemetry-computer system.

3. 48 bits
4. Time word frozen by time hold signal
5. Time readout initiated by time present signal

CDC 160 computer system:

1. General purpose, solid state, computer
2. Run and step modes
3. 6.4-microsecond memory cycle time
4. 12-bit computer word, signed
5. Parallel logic
6. 67 instructions
 - a. Manipulatory
 - b. Arithmetic
 - c. Jumps
 - d. Input/output
 - e. Miscellaneous
7. 4096-word, magnetic core storage
8. Nonbuffered input/output

Peripheral equipment of telemetry computer system:

1. Four magnetic tape transports
 - a. 150-ips speed
 - b. 200 lines per inch
 - c. 30-kc character rate
 - d. IBM compatible
2. Typewriter
3. Paper tape reader
4. Paper tape punch

Figure 4 is a general block diagram of the integrated telemetry-computer system showing the connection lines between the various subsystems. The data flow is shown by the heavy black

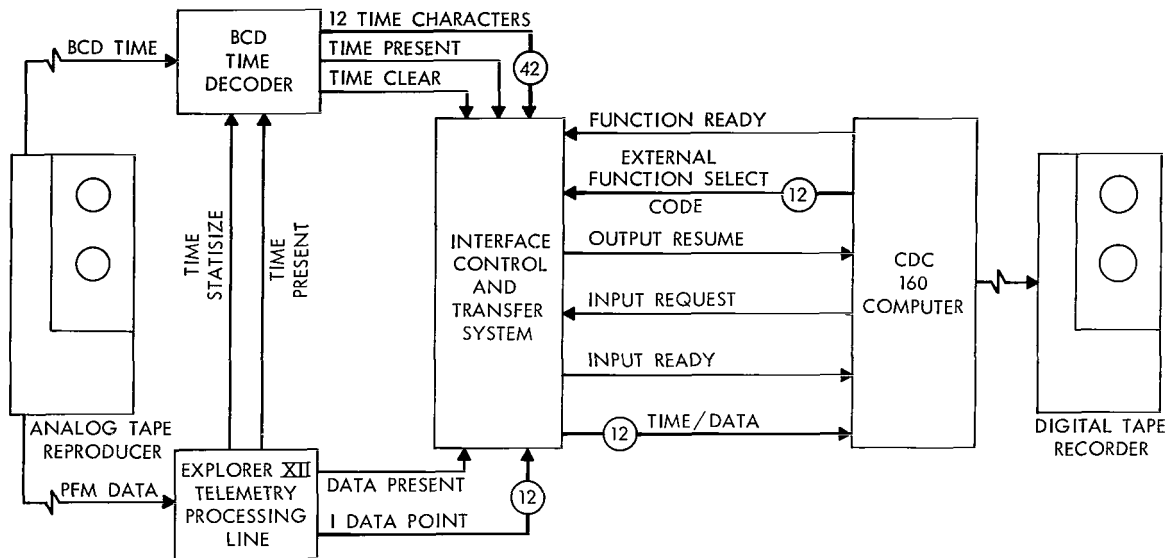


Figure 4-Diagram of integrated telemetry-computer system showing connections between various subsystems.

lines and the control functions, by the lighter lines. All data and control paths flow from left to right in the diagram with the exception of those connecting the computer, which has to communicate bidirectionally. The sequence of events up to the interface circuits of the control and transfer subsystem is relatively straightforward. PFM data are reproduced on one channel of the analog tape reproducer and are sent serially, bit by bit, to the S-3 telemetry processing line for conversion to digital form. At the same time, BCD time is read from another channel to the BCD time decoder. The main points for design consideration are presented below.

Timing

The timing constraints are as follows:

1. Input cycle: The computer cycle time is approximately 3000 times faster than the telemetry data rate of 20 milliseconds.
2. A typical, uncomplicated load and store series of instructions can be performed in 28 microseconds. Therefore, information can be moved nearly 700 times between data inputs.
3. No timing constraints are imposed by the computer on the data input.

Data Input

The data input information is:

1. Synchronization pulses are generated every 20 milliseconds for a data word and every 320 milliseconds for frame recognition.
2. Bad data flags are generated.
3. Error possibilities are:
 - a. Too many data words per frame (17 or more). When this occurs the extra words must be locked out.
 - b. Too few data words per frame (15 or less). When this happens, extra words need to be added to fill out one frame.

Time Input

The time input requirements are:

1. 12 BCD characters; hundreds of days down to units of milliseconds.
2. Time; transmitted 7.5 milliseconds after the last data point per frame occurs.
3. 48 bits to be transferred each time.
4. Time is transmitted every 320 milliseconds.

Output From Computer to Magnetic Tape

At end of a 960-time-and-data-character input (16 frames), an output is necessary. The timing requirements of magnetic tape transports are:

1. Write time - 33.5 microseconds per character; total block storage is approximately 33 milliseconds.
2. Magnetic tape transport turn-on time:
 - (1) 20 milliseconds to move off the load point;
 - (2) 20 to 35 milliseconds to obtain recording speeds depending on the unit.
3. Best output time is approximately 53 milliseconds, not considering safety factors or programming extras.

Computer Constraints

The computer places constraints upon the system along with the magnetic tape drives because:

1. It lacks buffering capability to interlace input and output cycles sequentially at fast data rates.
2. It must select a piece of external equipment and hold that selection until the input/output process is completed.
3. No computation can take place when the computer inputs or outputs blocks of data.

Once synchronization is obtained in the processor, the data words are processed by the Explorer XII telemetry processing line and a digital data word is sent in twelve parallel bits to the interface control and transfer subsystem (ICTS). Each data word is accompanied by a data present pulse to signify its presence in the processor output register. The ICTS does not accept the data words until frame synchronization has occurred.

At sync time the 16th data word of a frame will have been digitized in the telemetry processor. The processor will send a "time statize" or a "time hold" pulse to the BCD time decoder to freeze a time word. Along with it will be a "time present" pulse which is used to generate a "time clear" strobe; it also passes on through the time decoder to the interface circuits to start a transfer sequence. Forty-two bits comprising twelve characters of time are then stored in the ICTS time storage registers awaiting passage to the CDC 160.

The computer takes in the time in 4 computer words of 12 binary bits. It then takes in 4 data words which have been stored at 20-millisecond intervals over a total period of 80 milliseconds. The data cycle is repeated a second, third, and fourth time over a frame period of 320 milliseconds. The frame time is the duration it takes for 16 words to pass through the processor for analog to digital conversion. This insertion of 20 words into the computer is the basic cycle and it is repeated 16 times until 960 time and data characters have been stored and an output cycle is required.

Depending upon the point in time in the processing sequence, either the ICTS or the computer can initiate the transfer between the units. The control sequence between the ICTS and the computer is started when the computer sends a "function ready" signal plus an "external function select" code of 12 parallel bits (an octal designation). This is the computer's way of isolating the ICTS from other external devices peripheral to the computer and prepares the computer input circuits to accept data from the ICTS. The ICTS returns an "output resume" pulse to the computer to notify it that it has acknowledged selection. The computer once again returns a control signal in the form of an "input request." This is examined by the ICTS and if time or data are ready to be transferred, an "input ready" is sent back to the CDC 160 which will then take in 12 bits of information.

The input cycle, once underway, consists of the 4 time words accepted by the computer with a time limitation dictated only by the amount of program requirements performed by the computer. The time input is followed by the acceptance of 16 data words in 4 subcycles of 4 data words each. The timing for the loading of the 16 data words is dependent upon the data rate as well as upon the internal program considerations. The ICTS collects 4 data words at a 20-millisecond rate for each input. At the fourth input, i.e., at a total elapsed time of 80 milliseconds, the ICTS notifies the

computer that data are ready to be sent to it. The computer reads in the four words, performs calculations, and returns to wait for the start of the next data subcycle.

When 960 time and data characters are stored the computer unloads the information in a record of 960 characters on digital magnetic tape. This input-output sequence is continued until processing is ended. Any incompleted block at the end is filled by a program subroutine and is stored on the magnetic tape to complete a record file. The initial control references between the CDC 160 and the ICTS will come from the computer at the start of a processing cycle and after each output record. The ICTS will provide the control enable between input frames while 960 characters are being stored in the computer prior to the output cycle. These signals can be either pulses or voltage levels depending upon whether the system is in the operational, the simulator run, or the simulator step mode.

Integrated Control and Transfer Subsystem

Data passage between the three major subsystems is dependent upon the integrated control and transfer subsystem. Upon development of this subsystem, the Explorer XII telemetry processor, the BCD time decoder, and the CDC 160 computer were joined together physically and operationally. A block diagram of the various parts of the integrated control and transfer subsystem (ICTS) is given in Figure 5. The ICTS consists of eight important circuit areas; these are shown within the blocks in Figure 5. The following paragraphs present a general description of the function each area performs.

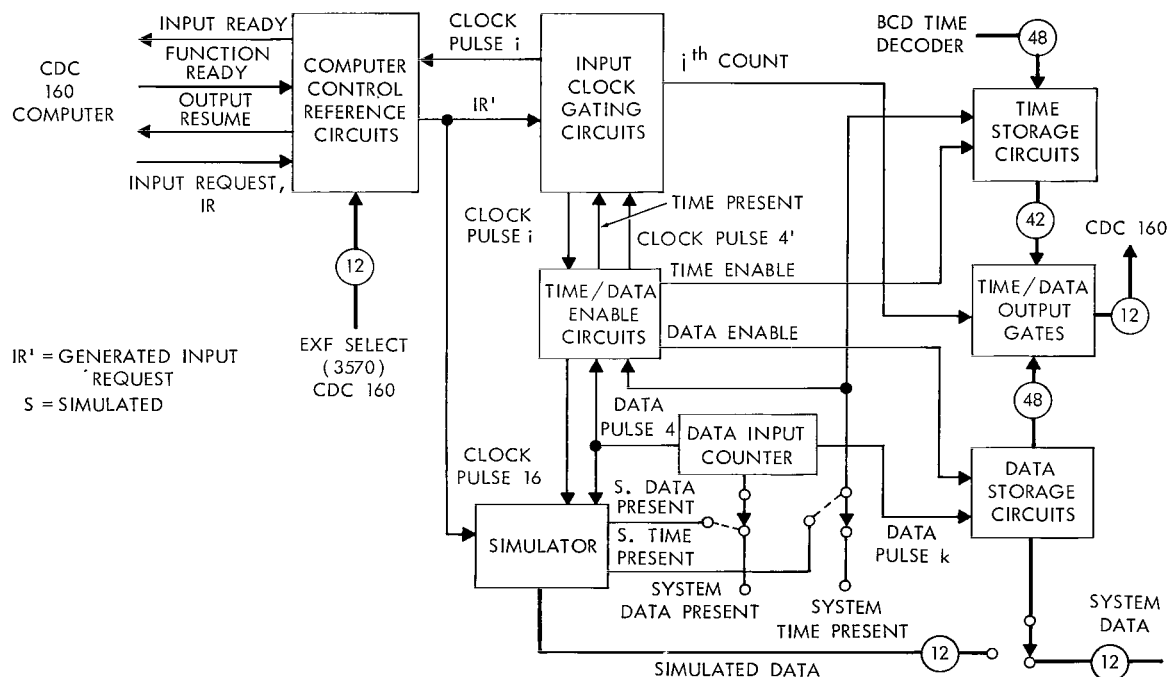


Figure 5-Integrated control and transfer subsystem.

System Run Mode

The system run mode is for the system operational process. The computer performs at its optimum cycle speed of 6.4 microseconds as it accepts, processes, and outputs the converted time and data information. The throughput rate of the system is determined by the input data rate, which for this design configuration is 20 milliseconds.

Simulator Run Mode

The simulator run mode is used for dynamic testing. In this mode, the control, timing, and transfer circuits are tested at a data rate the same as the system rate when it is processing information. The data are repetitive for all characters in a frame. Sequencing is initiated by the computer. The simulator isolates the processor as a source of error, and also the time decoder, if desired.

Simulator Step Mode

The simulator step mode is used for static checks. Its primary function is to check the contents of the transfer circuits' storage registers. Level settings on the control elements are also tested. The simulator step mode is also used to step sequentially through the computer instructions that are necessary for communication between the computer and the integrated transfer and control system.

PROGRAMMING REQUIREMENTS

The following are program requirements for the system while processing the Explorer XII data tapes. The computer must accept 12 characters of time, which constitute four time words, at 320-millisecond intervals, and one character of data every 20 milliseconds. Another necessary function is the outputting of a 960-character block approximately every 5.1 seconds. The computer is also required to convert the code for BCD zero, as well as to insert three special BCD characters for erroneous data.

The operations the computer performs are as follows:

1. Accepts 12 time characters at 320-millisecond intervals.
2. Performs BCD-binary conversion on the milliseconds of time.
3. Separates time words into 12 characters; program multiplexing is used for this.
4. Corrects for BCD zero on time inputs.
5. Accepts four data words every 80 milliseconds; these are four 12-bit words.
6. Separates data words into three characters; program multiplexing is used for this.
7. Corrects for BCD zero on data inputs.
8. Outputs 960 character blocks of information.

In addition to performance of the above operation, the following quality control functions are also conducted:

1. Performs a time differential check on milliseconds of time.
2. Flags bad time.
3. Stores initial time.
4. Limit tests for bad data words.
5. Flags bad data words.
6. Counts bad data words.
7. Counts frames of data.
8. Performs "quasi-clock" search - a complex operation (see section entitled "Quasi-Clock Cycle Subroutine").
9. Extracts "quasi-clock" information.
10. Performs RIDL cycle search - a complex operation (see section entitled "RIDL Cycle Subroutine").
11. Extracts RIDL cycle information.

Approximate Execution Times for Processing Subroutines

The approximate execution times for the processing subroutines are given in Table 1. Times are given for the time, data, RIDL cycle, and quasi-clock cycle subroutines. The RIDL and quasi-clock cycles are described in paragraphs bearing those titles in the section entitled "Program Flow Charts."

Program Functions

The program subroutines performed the following functions during the data flow process:

1. Input and storage of time and data.
2. Data flagging ordinarily performed on special purpose equipment.
3. Quality checks performed during subsequent computer operations.
4. Determination and extraction of subcommutated data cycles performed during post-processing computer operations.

Table 1

Approximate Execution Times
for Processing Subroutines

Time subroutine	
Input of 12 time characters (4 time words)	2 ms
BCD to binary conversion	
Initial	2.8 ms
Final	300 μ s
Check for time difference between two words	220 μ s
Initial time storage T_i	1.7 ms
Data subroutine	
Input rate for 1 data point (3 BCD characters)	
Good data point	280 μ s
Bad data point	500 μ s
Output rates for 1 data point (3 BCD characters)	
3 BCD characters (1 computer word) . .	12.8 μ s
Magnetic tape write time per character	33½ μ s
Total 960 character write time	33 ms
Tape turn-on time	20 ms
Total output time	53 ms
RIDL cycle subroutine	
Switches in and out during every frame and tests for values, maximum time	40 ms
12 character time transfer	1.2 ms
Quasi-clock, missing data points/RIDL cycle, missing frames/RIDL cycle . .	400 μ s
Data point 15	53 μ s
Total time	2.17 ms
Quasi-clock cycle subroutine	
The composite estimate at maximum number of sequences	1.5 to 2 ms

5. Output editing and formatting of time and data.
6. Output editing of quality control and extraction of supercommutated data for specific experiments.
7. Program "housekeeping" to retain control and organization of the data flow process.

These functions are shown according to their sequence of occurrence in the program flow diagrams.

Program Flow Charts

The flow charts of the integrated telemetry-computer system are presented in the following order: The general data flow, general throughput buffer mode, identification subroutine, time subroutine, data subroutine, RIDL cycle subroutine, quasi-clock subroutine, file stop time and block fill, and printout routines.

Time and Data Processing Sequence

The programming for the computer integration project was carried out as the hardware development progressed. The following stages of program construction were considered. First, the basic subroutine called for an input of a 12-character time word followed by 16 three-character data words. This arrangement was repeated for 16 time frames until a storage block of 960 characters was accumulated. At the completion of the block storage, an output of all 960 characters to magnetic tape was required. This basic throughput mode is shown at the top of Figure 6.

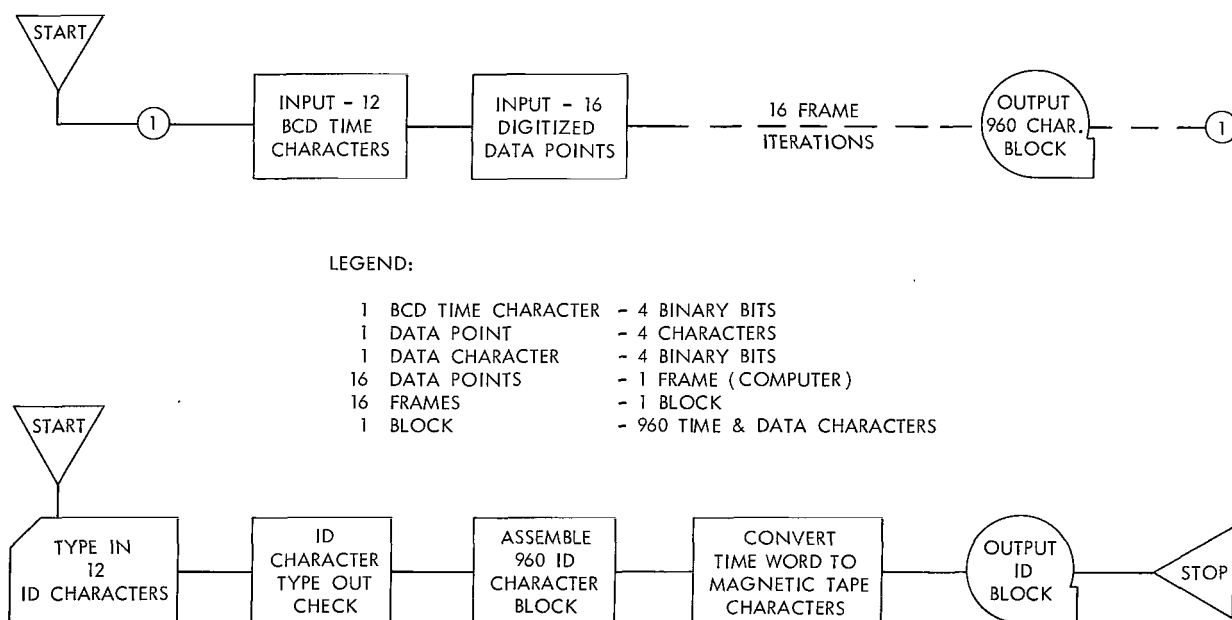


Figure 6-Time and data processing sequence (buffer throughput mode) and identification (ID) subroutine.

Construction of the integrated telemetry-computer system was based on a 12-character BCD time word to be read in before data was stored. After reading in the time word, the computer was constrained by the system to accept 4 groups of 4 data words at intervals of 80 milliseconds rather than 16 data words at 20-millisecond intervals each. The time read-in intervals were spaced at the data frame rate of 320 milliseconds. An output block of information occurred every 5.12 seconds.

The identification subroutine at the bottom of Figure 6 is performed prior to tape processing, and the ID information will always be the first block on any digitized tape.

Time Subroutine Flow Chart

Accepting time from an input source and checking time within the CDC 160 computer are performed as shown in the time subroutine flow chart (Figure 7). Whenever a frame of data is to be inserted into the computer, it is preceded by a 12-character time word. When the time word is stored in the time storage register of the interface control and transfer system circuits, a time present signal is generated that notifies the computer to accept it. The CDC 160 then transfers the 12 characters and divides them into 3 binary-coded-decimal character words. Once in the computer, each of the characters is isolated and a test for a binary coded decimal (BCD) zero is made.

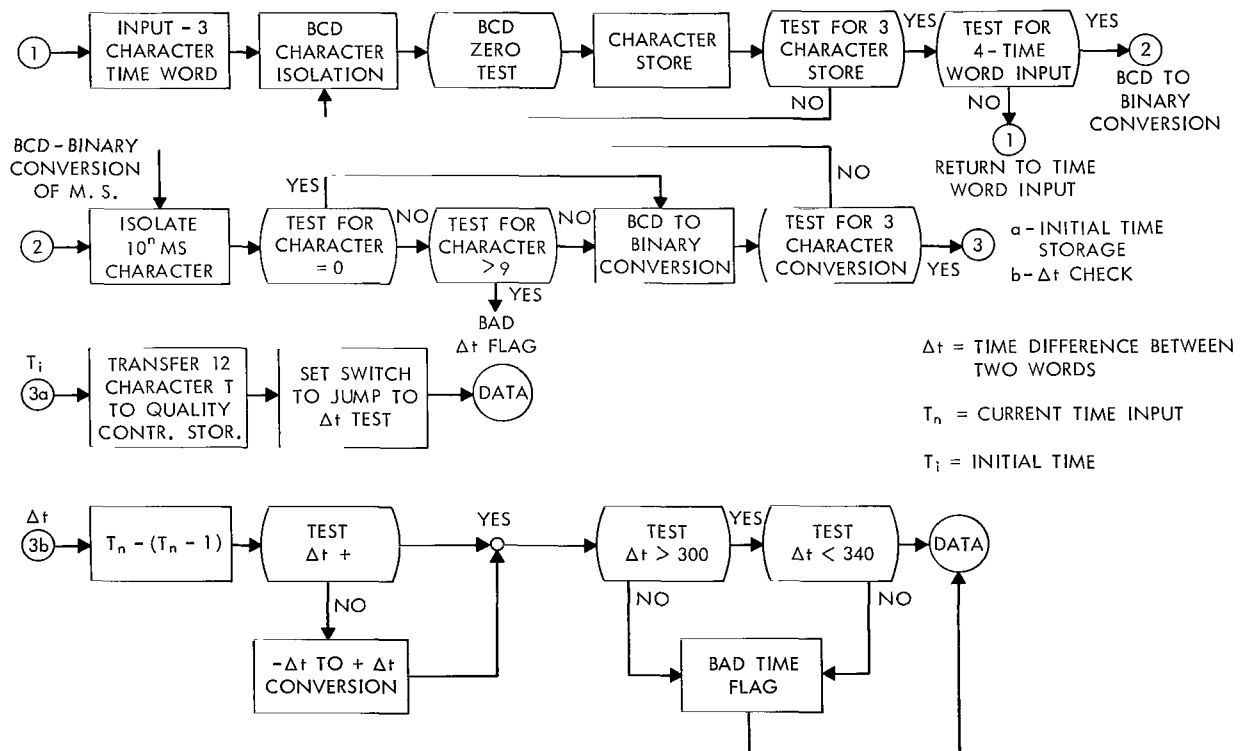


Figure 7-Time subroutine flow chart.

No provisions were made in the circuits of the system to convert a binary zero to a BCD zero. This was a hardware function of the special purpose format buffer used in the processing lines shown in Figure 2. The computer must handle this test through programming. This conversion is necessary for later parity checks and character translations.

The program then stores a character, tests it to find out if three characters have been checked and, if not, repeats the three character strip-out. Afterwards the program tests for four time words, returning to the input until a complete word is loaded.

The next task is a conversion of the millisecond portion of the time word from three BCD characters to a 12-bit binary word in preparation for a quality check of the time differential (Δt) between two frames of data. The BCD-binary conversion is shown between points 2 and 3 of the time subroutine flow chart. The program first determines the characters by powers of ten. It tests the extreme digits, 0 and 9, of the decimal radix and converts each BCD character to a binary representation. A three-character test follows and is necessary to provide for a summation of characters for units, tens, and hundreds of milliseconds.

Once the conversion is completed the computer has to ascertain if the time input is the initial time transfer of the production run. If it is the initial time (T_1) then no millisecond check can be made. The computer program then performs a switch routine to allow Δt checks for any following time words and transfers control to the beginning of the data input subroutine.

For all other time inputs, the subroutine jumps into a Δt check. The computer subtracts the previous time input ($T_n - 1$) from the current time input (T_n). A check is made for a positive or negative differential to account for a millisecond update greater than 1000 which will appear as a lesser number, since 999 is the highest possible millisecond count. If this is the case, the program computes the residue mode to 1000 and then a limit check is performed to determine if the time differential is 320 milliseconds plus or minus 20 milliseconds. This is done by testing the lower limit at 300 milliseconds and the upper limit at 340 milliseconds. If the difference exceeds these limits, a bad-time flag is placed in the second time word in storage. Housekeeping resets and relocations are performed at the end of each time pass prior to entering the data subroutine.

Data Subroutine Flow Chart

The subroutine for the collection and storage of data would be a simple one except for special experimenter processing requirements. In the simplest case data would be brought into the computer and stored. The program would tabulate data points for the output cycle and return to the time input or to a routine to output after a block of 960 characters had been stored. As can be seen in the data flow chart (Figure 8), this was not the case. Several checks similar to those performed were required on each time word for data inputs. As each data word arrives in the computer, it is tested for an upper limit to determine its worth to the experiment. If it is not valid, three bad-data word flags are placed into character storage for each data word. The number of bad data points are accumulated for later editing and quality control functions. When the data word is acknowledged to be valid by the computer, each data character is masked out, a BCD zero test

is performed, and the character is stored in the 960 character block storage. After storage of each character, a test is made to make certain each of the characters of the word have been placed in memory. When a word storage is completed the computer brings in the next data word.

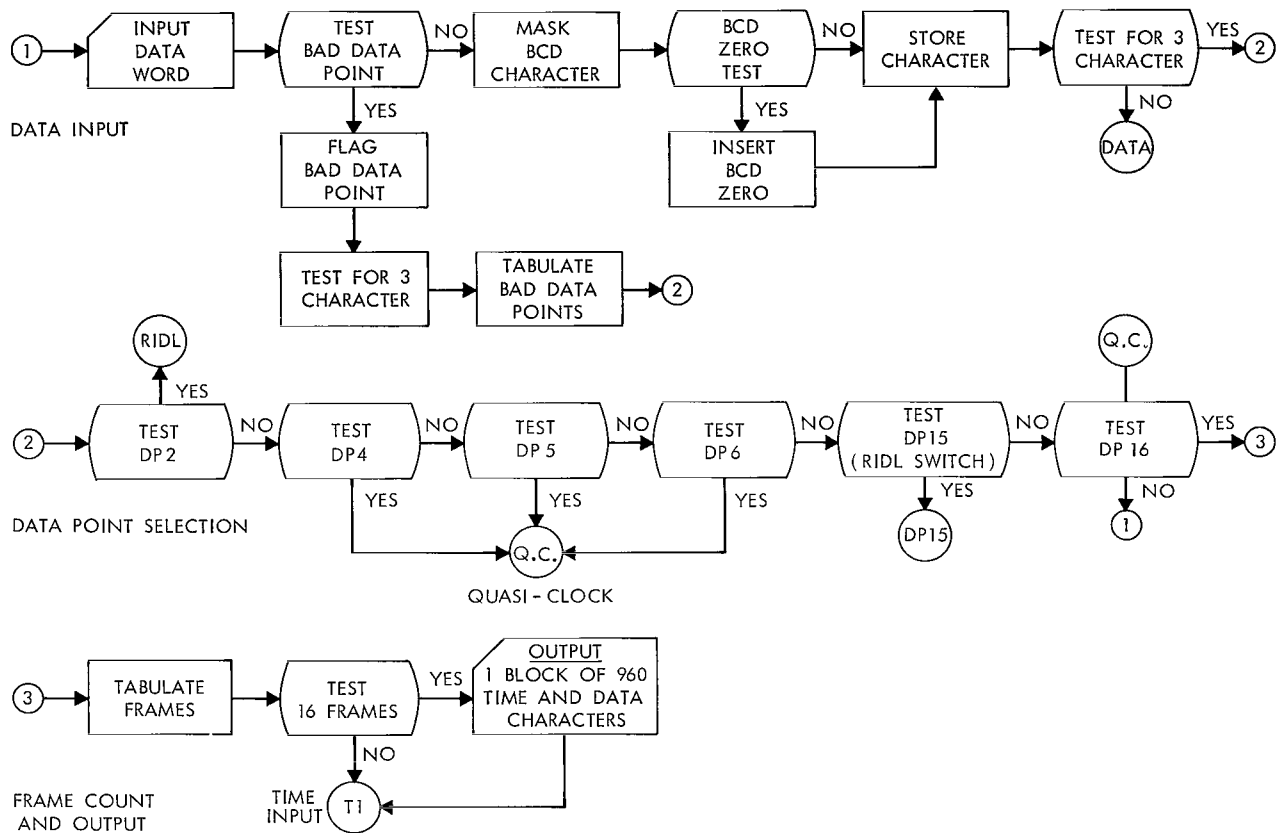


Figure 8-Data subroutine flow chart.

The program handles each data input to the external storage. The program first determines the mode of data input: sixteen data words in blocks of four from an external register or one data word at a time. The computer can operate more expediently on four data words and consequently wait longer for more data inputs. In either case, as was previously pointed out, the requirements for checks at input involve very little time compared with the time interval between data words. The programming discussed is shown from point 1 to point 2 of the flow chart.

Additional programs demonstrated the feasibility of concurrent computer processing during the digitizing phase of production. Without them the data subroutines would have been terminated by the subroutine shown starting at point 3 of the flow chart, the frame count and output program. This program tabulates the number of frames accepted by the computer and tests for storage of sixteen frames, consisting of 960 time and data characters. If less than sixteen frames are stored,

an incomplete block is signified and control is switched for another frame cycle starting with a time input. When the block is filled, an output commences and a block of information is recorded on digital magnetic tapes. At the completion of the output cycle, the program returns to the time input subroutine.

When one looks back to the data subroutine flow chart at the point 2 input for data word selection, one can see that a number of auxiliary program exits have been inserted. This is the method used for extraction of experimental information pertinent to given channels. Provisions have been made to bypass individual routines if they are not recognized. This causes the program to branch to an auxiliary path and to continue through the data flow previously mentioned.

As each data word is loaded into the CDC 160 computer, a test is made to determine at what point in a frame it is to be located. Data word 2 recognition calls for a branch to search for super-commutated data used for an experiment designated the RIDL cycle. Data words 4, 5, and 6 are used jointly to determine another experiment called a quasi-clock cycle. The data word 15 is also recognized in conjunction with the RIDL cycle test. Data word 16 is used as the key for determining frame and block counts.

No details will be given concerning the nature of the experimental data in the programs. The emphasis will be placed on the processing requirements and the method of implementing the program to recover the data.

RIDL (Radiation Instrument Development Laboratory) Cycle Subroutine

The steps required for recovering the data are as follows:

1. Check each frame for DP 2 (here DP stands for "data point" and is synonymous with data word).
2. Test for DP 2 equal to 200.
3. Test for eight consecutive DP 2's equal to 200.
4. Test for DP 2 equal to 400.
5. Read RIDL cycle time.
6. Count frames per RIDL cycle.
7. Count eight DP 15's.
8. Store eighth DP 15.

In satisfying the above requirements, the computer program must make a number of complex decisions, and a number of supplementary functions are also performed. It can be seen from the RIDL cycle subroutine flow chart (Figure 9) that the program first tests for DP 2 after branching from the main data flow path and then tests the quantity of the data word. If the data point equals 200, the RIDL cycle continues by switching the sequence from the test just completed to another subset with entry at point 3 to test for eight consecutive DP 2's. If not, the program merely returns to the normal data flow path. When eight data points are counted and another test for 200 is verified then the next data point is tested to see if it equals 400. If any of these tests fail, resets

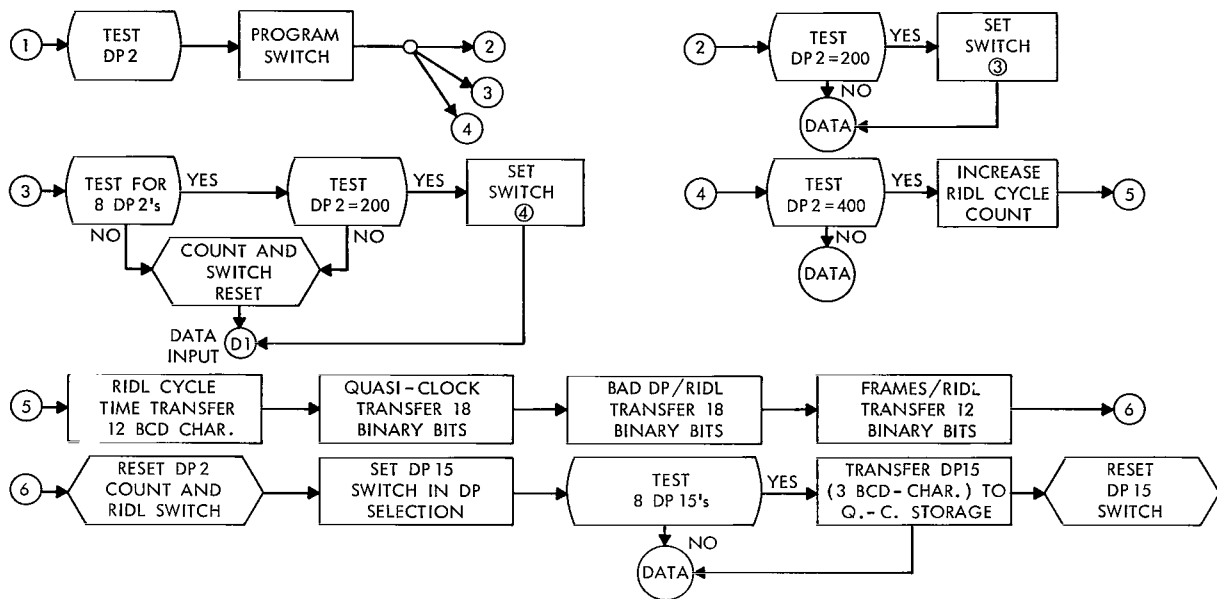


Figure 9-RIDL cycle subroutine flow chart.

are made and the program reinitiates a new search mode. When the value is found to equal 400, the RIDL cycle is identified and a count made of the cycles. These cycles occur approximately 7.5 minutes apart on the Explorer XII Satellite.

After the RIDL cycle is determined the program enters point 5 on the flow diagram and then transfers the 12 most recent characters of time to a storage block used for experiment and quality control information, transfers 18 binary bits of quasi-clock information that had been temporarily stored by the quasi-clock subroutine, and transfers a count of bad data points and the number of data frames which occur during the RIDL cycle. At this point the computer resets various program switches, counts eight DP 15's, and transfers the eighth DP 15 to the RIDL storage block. The sequence of events is illustrated from point 6 on the flow diagram to the return to the main data flow. Whereas all of the above program decisions are placed in the RIDL cycle subroutine, the DP 15 test is placed in the main data flow path to eliminate complicated interactions with the DP 2 flow paths.

Quasi-Clock Cycle Subroutine

The quasi-clock cycle was a method to utilize known quantities of the data format to extract time information since no clock word was included in the format. The determination of the quasi-clock cycle is a complex programming problem and is even more difficult when associated with a real time data collection and conversion system. The program had to first detect both supercommutation and subcommutation sequences before extracting the required data.

The quasi-clock data was transmitted from telemetry channels 4, 5, and 6 of Explorer XII. The clock increased a count of one after 240 frames of data. The cycle format was composed of

four identical 60-frame subcycles with the quasi-clock count appearing either twice or eight times during the main 240-frame cycle.

The program for extracting the quasi-clock information is shown in Figure 10 and is described as follows:

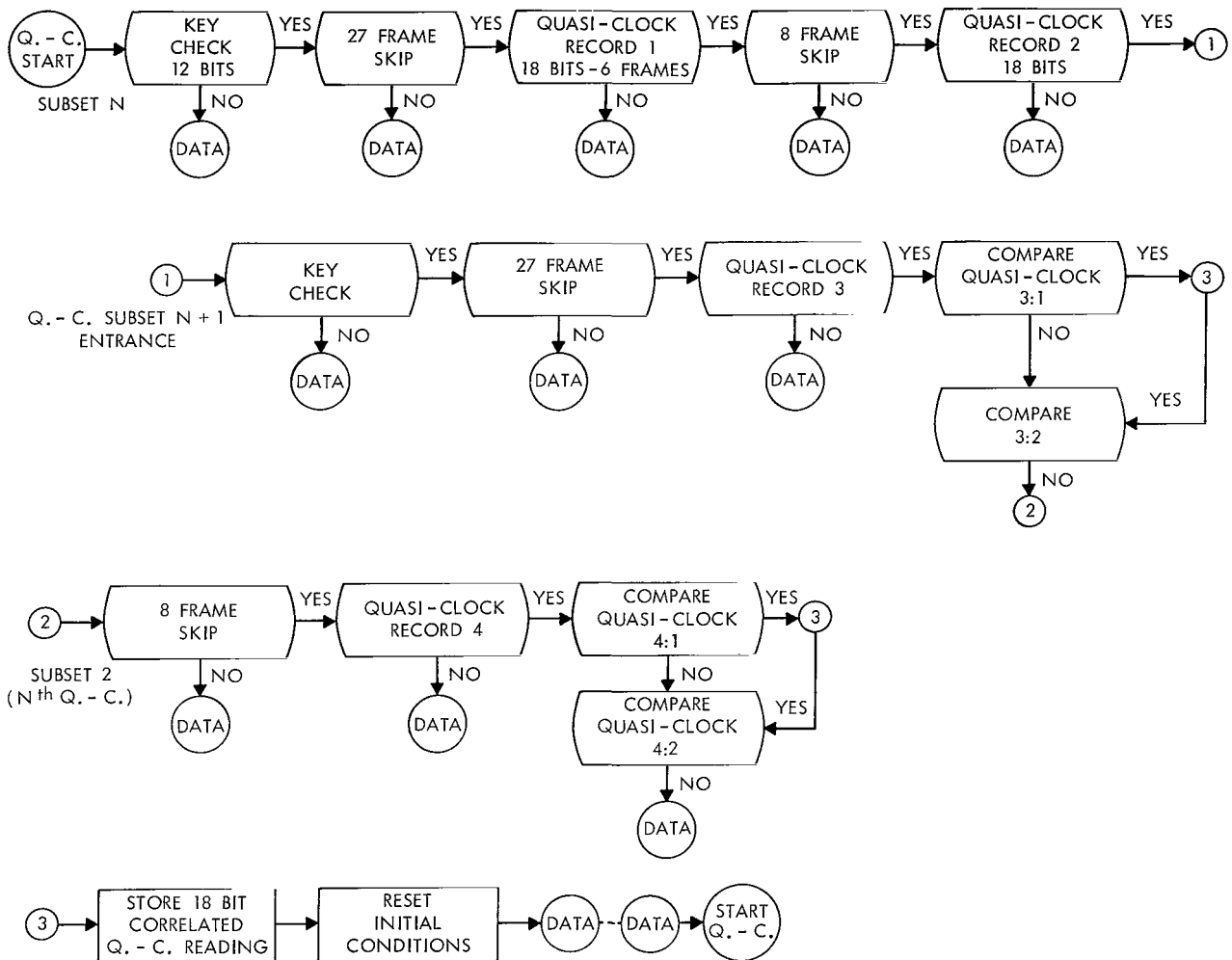


Figure 10-Quasi-clock cycle flow chart.

1. The program finds a 12-bit synchronization key consisting of the lower bit in the upper data character of a data word from 12 consecutive frames. This key is extracted from 12 consecutive frames from channels 4, 5, and 6. These frames are always the first 12 frames of each 60-frame subset. The synchronization key is recognized by comparison with a known bit pattern stored in the computer. The computer will accept the first valid pattern that appears in one of the three channels.

2. The program counts 27 consecutive data frames for a second extraction of data.
3. The program extracts the first quasi-clock reading of 18 bits of each 60-frame subset. These consist of six bits from data words 4, 5, and 6 from six consecutive frames. The bits again consist of the lowest order bit of the upper data character in each data word.
4. An 8-frame skip is performed and the second 18-bit quasi-clock record of the 60-frame subset is extracted.
5. A positive identification is made by finding a correlation between two quasi-clock extractions from eight different subsets. This can be seen in the quasi-clock comparisons in the flow diagram which illustrates the conditions for subsets 1 through 4. The routine searches through the four subsets, or subcycles of a 240 frame sequence, making a check for 20 possible correlations.
6. After the quasi-clock is confirmed by cross correlation technique, the 18-bit quasi-clock word is stored for future use. The transfer of this clock count to a quality control storage location is performed along with the transfer of information obtained during the RIDL cycle. Since the quasi-clock occurs every 240 frames of approximately 1 minute and 17 seconds, it can be considered as a minor wheel rotation inside the 7.5 minute RIDL cycle. The quasi-clock will update nearly six times within a RIDL cycle under normal conditions. The quasi-clock program "free wheels" until the larger cycle of the RIDL period is completed, and then its most current reading is stored. The 18-bit quasi-clock storage is reset to eliminate the possibility of reading out erroneous data because of the asynchronism between the quasi-clock wheel and the RIDL cycle.

Storage of File Stop Time and Printout of Final Block

When processing of analog data is complete, a number of statistics must be derived. The final time for the last full frame of data must also be recorded and any incomplete block of data must be filled for proper block length on tape.

The flow diagram in Figure 11 illustrates the above operations. The computer locates the last storage address used, transfers the final time word to a quality control storage area, and fills the remaining storage cells of the 960-character block with bad data flags. The final block is loaded on magnetic tape, and an end-of-file is written to indicate where loading stopped. The run is completed by rewinding the magnetic tape and printing out "End of Run." This post-processing routine is completed immediately after a conversion of analog to digital data.

Quality Control Printout

When the production run is completed, a digital magnetic tape is available for decommutation or further analysis which can be done immediately by off-line processing programs. In any case, the magnetic tape can be used for further processing or data can be printed directly on the typewriter in 960 character blocks.

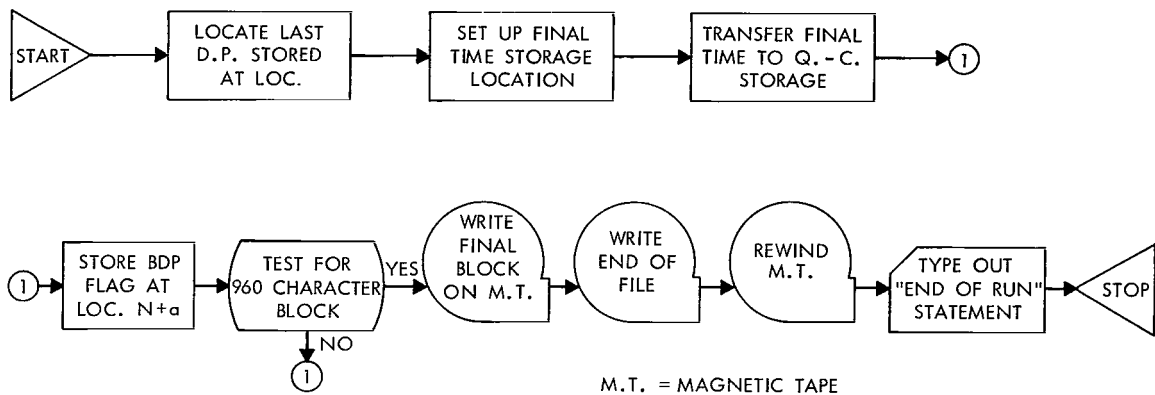


Figure 11-File stop time storage and final block fill flow chart.

Prior to performing the block printouts, the computer program calls for a printout of all the previously stored statistical and quality control information. The printout subroutine is shown in Figure 12. Since the information is collected and retained in both BCD and binary number formats during processing and the different input/output routines call for various equipment coding, extensive program effort for character conversion, translation, and information movement was required.

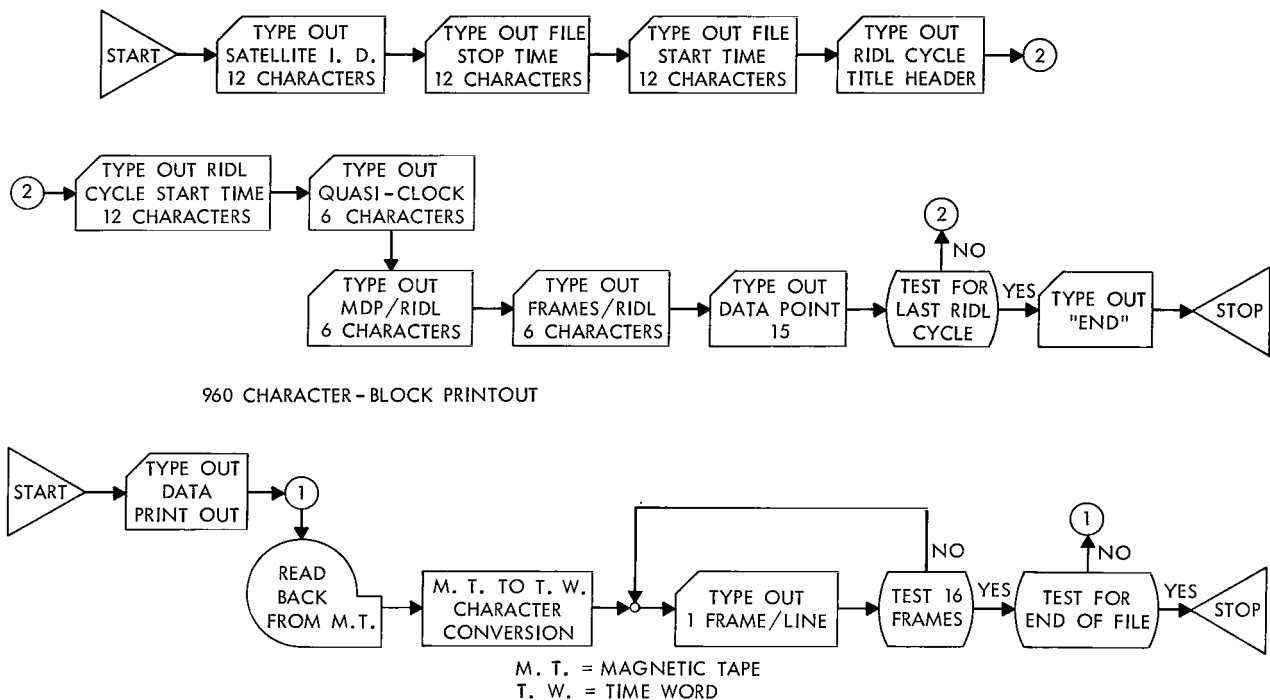


Figure 12-Quality control printout flow chart.

SOFTWARE INTEGRATION

Data Processing Alternatives

When a computer is part of an overall system, two alternatives are available for data processing. The first alternative is a two-pass operation. During the first pass, the computer can be used as an output buffering device. The computer can accept, store, and transmit data to a magnetic tape. The magnetic tape can then be rewound and played back for quality control calculations and editing by the computer during the second pass.

The second alternative is a one-pass operation which consists of a simultaneous performance of the buffering process together with data quality control. In the one-pass operation, the time intervals between data inputs can be used for data manipulations and for quality control calculations. The computer is thereby put to work more efficiently during a given time span. This comprehensive approach is the preferred one.

Support Parameters

A general purpose computer, even of small scale, can be used for one-pass operations of telemetry data if it has an adequate instruction repertoire and rapid cycle times. A computer with buffered input/output can easily accomplish all quality control requirements on data input rates of a slow and medium nature. In the case of very fast data rates, iterative time-consuming functions such as data synchronization, binary coded decimal-to-binary conversions, and limit checks should be handled externally to allow for other computations.

As this project has proven, a nonbuffered computer can be used for on-line processing; however, this type of system is nearly always output limited if data are to be transferred to magnetic tape. Costs for computer interface equipment can be absorbed more easily in the purchase of a buffered computer. Furthermore data processing "system variability" is difficult to achieve with a non-buffered machine. System variability can best be achieved in a buffered system through programming.

Future Design Concepts

A desirable feature of future systems will be closed-loop program control, that is, a capability to feedback information to the telemetry processor. With this capability telemetry processors will be controlled by the computer. Extending the communication process is the next progressive step to be taken for the integrated telemetry-computer system. The computer should be enhanced so that it controls the satellite data rate format and techniques should be developed to synchronize the data stream properly. The computer should also be capable of providing servo control for better resolution of raw data signals.

CONCLUSIONS

The conclusions derived from the telemetry-computer integration project are as follows: The design was tested and proven to be feasible. The results obtained from the engineering efforts of the design project led to further overall conclusions, beyond the scope of the design project, that the advantages and disadvantages of various computers can be assessed with regard to present and future telemetry reduction systems. Specifically, it was shown that by coupling a computer to the output of a telemetry signal processing line in place of currently used buffering devices, immediate savings in time, manpower, and efficiency result. In addition, the following improvements are accomplished:

1. The computer replaces the special purpose equipment and eliminates "duplication of function" costs.
2. Magnetic tape recording equipment and storage space for reels of tape containing intermediate processed data is eliminated.
3. Manpower and transportation costs for movement of the magnetic tapes are removed.
4. Time compression in the total data processing cycle is achieved. Analog processing, physical tape movement, and computer analysis are incorporated so that all three functions are performed during the analog processing time.

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